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Measurements of thermoelectric properties of silicon pillars

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ABSTRACT

Nanostructured silicon as a material for thermoelectrics provides several advantages over conventional materials, such as bismuth telluride or lead telluride. The technological processing of silicon is well advanced due to the rapid development of microelectronics in recent decades. Silicon is largely available and environmentally friendly. The operating temperature of silicon thermoelectric generators is higher (>250 °C) compared to bismuth telluride. So far silicon is rarely used as a thermoelectric material because of its high thermal conductivity. The figure of merit Z, which is the commonly used measure of the thermoelectric properties of materials, is thereby too small for device applications. In order to introduce silicon as an efficient thermoelectric material thermal conductivity has to be drastically reduced. Nanostructuring into wires, i.e. restriction of the device geometry in both dimensions perpendicular to the heat propagation path indicates a route towards lower thermal conductivity. In this study we investigated silicon pillars produced in a wafer-scale top-down process by ICP (Inductive Coupled Plasma) cryogenic dry etching followed by thermal oxidation and oxide stripping. The pillars have diameters from 2 μm down to 170 nm. Their heights vary from 26.7 μm to 32.1 μm. We measured the reduction of thermal conductivity due to decreasing of pillar diameter. 3ω measurements were performed using a Wollaston probe with pillars of diameters down to 700 nm showing a reduction of thermal conductivity of 27% compared to bulk silicon.

1. Introduction

About 90% of the commercially available thermoelectric modules are manufactured from bismuth telluride. The efficiency of these modules, so far, was in the range of 6–8%. To improve the efficiency of thermoelectric devices it is necessary to improve the thermoelectric material properties towards higher ZT, with $Z = S^2\sigma/\kappa$ where T is the temperature, S is the Seebeck coefficient, σ and κ are the electrical and thermal conductivity, respectively. Classical thermoelectric materials like Bi_2Te_3, PbTe or SiGe achieve approximately $ZT \approx 1$ at 400 K, 650 K and 1200 K, respectively. After decades of stagnation nanostructuring of thermoelectric materials gives new hope for significantly improvement of efficiency of thermoelectric materials. ZT values of 2.4 and 3.5 caused by nanostructuring were reported [1,2]. For better ZT both Z and the temperature have to be increased. In addition, for many applications operation under fast changing temperature loads has to be managed, which occur, e.g. in the exhaust system of a motor vehicle. Extensive basic research is under way to achieve the required mechanical stability and good thermal contact to the heat source [3]. Unfortunately, bismuth telluride is not appropriate as a material for the corresponding, extremely interesting temperature range between 400 °C and 800 °C. One approach to improve the ZT factor of silicon is alloying with germanium. However, due to the limited availability of germanium at much higher cost with respect to silicon SiGe may be less attractive for high-volume applications.

Bulk single-crystalline silicon combined with a high-temperature-resistant joining technique based on pressure-assisted silver sintering is attractive for die-attached devices to be operated at high temperatures and temperature gradients [4]. Due to its high thermal conductivity, so far, bulk silicon was not considered as an efficient material for thermoelectric applications. However, silicon structured into wires of 100 nm in diameter or less exhibited a drastically reduced thermal conductivity. Values of ZT between 0.2 and 0.6 at 300 K were recently reported [5,6]. Conventionally, silicon nanowires were fabricated using self-organized vapour-phase deposition techniques which were developed for basic research in the lab. Top-down approaches, however, using wafer-level processing including lithography and anisotropic etching allow a reproducible fabrication of silicon pillars of uniform diameter and height. The latter is essential for simple electrical contact formation to pillar arrays.

It was expected that silicon nano pillars were difficult to be packaged within planar surfaces. However, first experiments to join the pillar arrays to a flat metallized surface (gold on sapphire) via pressure sintering joining technique were done successfully

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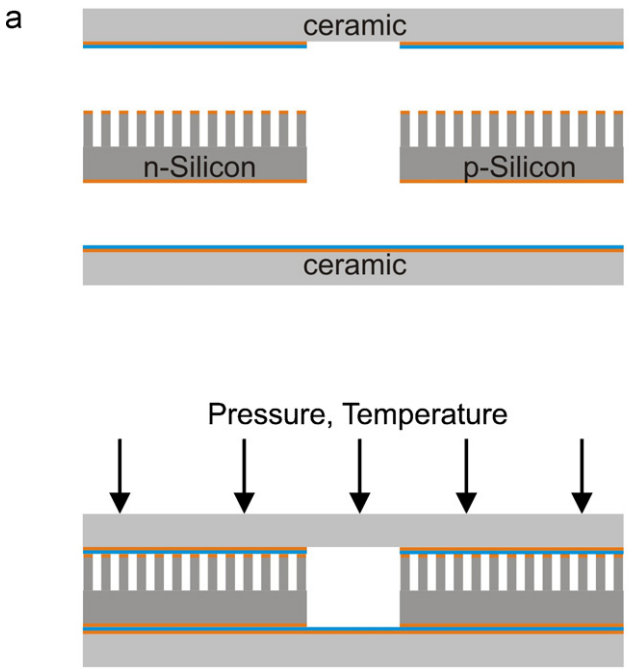

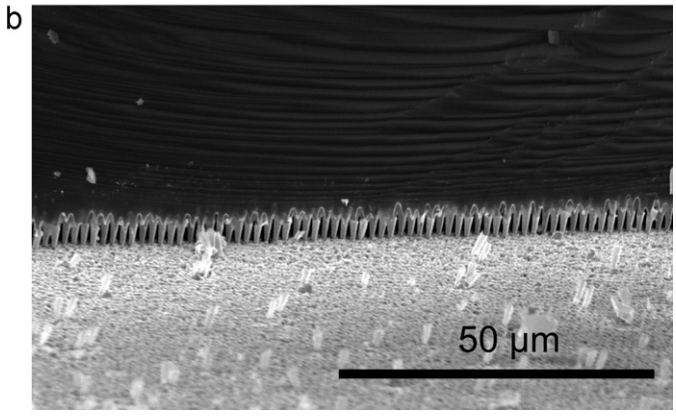

Fig. 1. Schematic of the sintering joining process of a thermocouple constructed by *n*-type and *p*-type silicon pillar arrays (a) and scanning electron microscope photograph of a pillar-to-substrate connection (b). For the displayed inclined cross-sectional view the sample was ruptured.

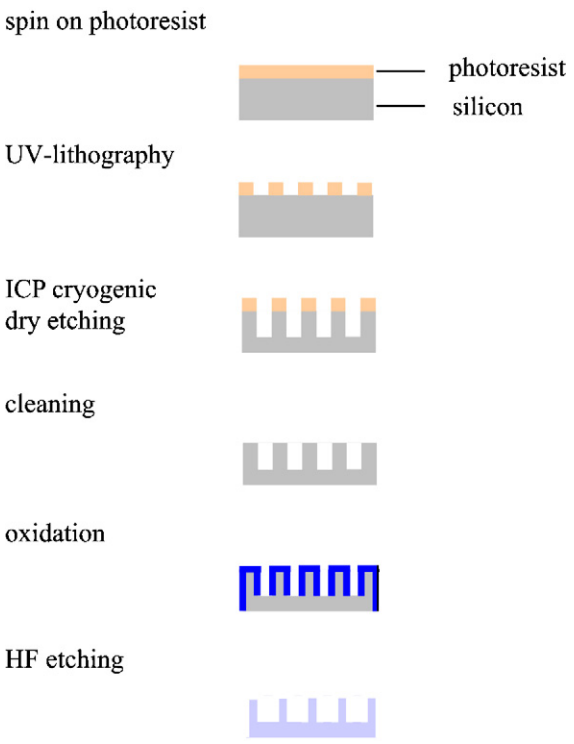

Fig. 2. Schematic of process flow for the fabrication of pillars in silicon.

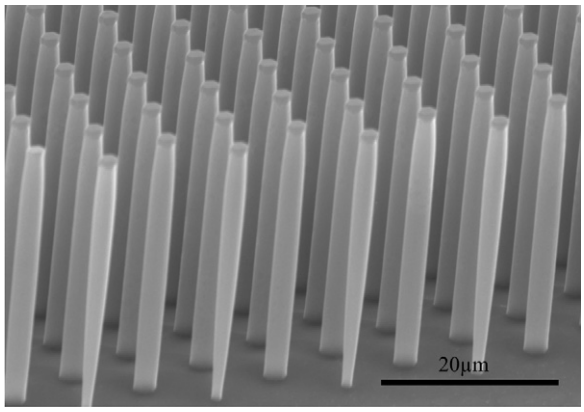

Fig. 3. Scanning electron micrograph (SEM) of ICP cryo etched pillars in silicon.

[7]. In this way ensembles of pillars in *n*- and *p*-type silicon can be processed and characterized in a controlled way. Therefore, with a top-down approach, the preparation of pillar arrays for thermoelectric characterization is considerably simplified, which is also attractive with respect to the design of future thermoelectric devices. Fig. 1(a) shows a schematic of the sintering joining process of a thermocouple constructed by *n*- and *p*-type silicon legs comprising pillar arrays. In Fig. 1(b) an inclined cross-sectional view of pillar array joined on a flat ceramic surface using pressure-assisted silver sintering is shown. For inspection in a scanning electron microscope the sample was ruptured confirming that the pillars were not affected by the joining process.

2. Fabrication of silicon pillars

2.1. ICP cryo dry etching

For the fabrication of pillars in silicon ICP cryo dry etching was used [8,9]. ICP cryo dry etching in silicon is an anisotropic process independent of crystallographic directions, in contrast to wet etching using alkaline solutions. Another advantage of dry etching is the possibility to use a photoresist instead of CVD (chemical vapour deposition) silicon nitride or thermal SiO_2 as an etching mask. Fig. 2 shows the process flow of nanopillar fabrication. Firstly, photo resist (AZ 726 MIF) is spun (3000 rpm) on the silicon wafer and structured using UV lithography. Photo resist masks (0.6 µm) were found to be stable during the following ICP cryo etching process for at least 0.4 h. The etching process duration was 230 s at −75 °C and a reactor pressure of 1.5 Pa in a SF_6/O_2 plasma. Using these process parameters pillars were generated having aspect ratios of more than 20 and diameters down to 400 nm. Fig. 3 shows a typical pillar array after ICP cryo etching. Constricted diameters at the bottom were only observed for the outermost row of the pillar array highlighting the effect of the pillar arrangement on the etching process.

Table 1
Reduction of pillar diameter by threefold thermal oxidation and subsequent HF etching tested with $N = 32$ samples.

	After ICP cryo dry etching	After first oxidation	After second oxidation	After third oxidation
n-Si	3.47 ± 0.03 μm	2.84 ± 0.01 μm	2.29 ± 0.01 μm	0.66 ± 0.02 nm
p-Si	1.57 ± 0.02 μm	0.75 ± 0.02 μm	0.38 ± 0.01 nm	0.16 ± 0.01 nm

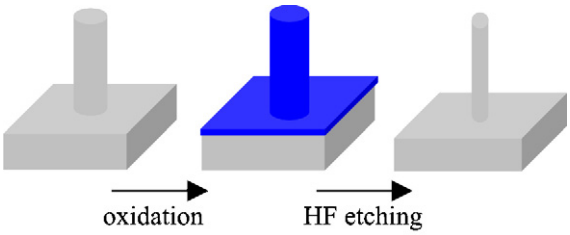

Fig. 4. Schematic of reduction of pillar diameter by thermal oxidation and subsequent oxide stripping in buffered HF.

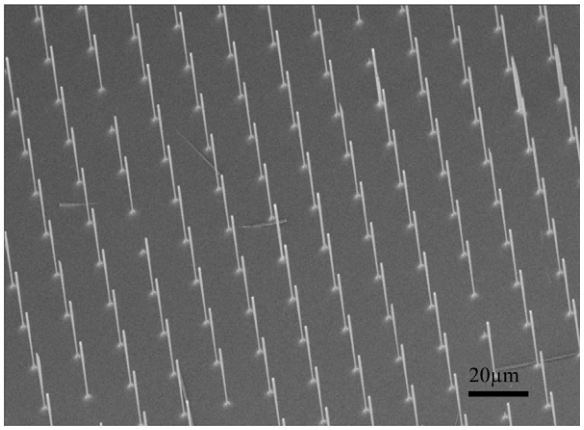

Fig. 5. SEM of *n*-silicon pillars after thermal oxidation and subsequent oxide stripping in buffered HF.

2.2. Thermal oxidation

A further reduction of the pillar diameter is accomplished by thermal oxidation followed by stripping of the oxide using buffered hydrofluoric acid (Etch Mixture AF, see Fig. 4). By reducing the pillar diameter a reduction of the thermal conductivity can be expected which then causes an increase of the figure of merit Z and thus the efficiency of a thermoelectric device. Thermal oxidation is highly reproducible process to generate a conformal sacrificial layer on a 3D silicon structure under uniform consumption of silicon which can then be removed at very high selectivity to the residual silicon. This step sequence was carried out three times resulting in a decrease of the diameter of the pillars by more than 2.5 μm. The results are summarized in Table 1.

Fig. 5 shows an array of *n*-silicon pillars after reduction of diameter by thermal oxidation and subsequent oxide etching in buffered HF. The area density of the silicon pillars was $1.6 \times 10^6/\text{mm}^2$ in an array with pillars of 400 nm in diameter and 400 nm pitch distance. This is in the range of densities published for black silicon needles (density: $(1–2) \times 10^6/\text{mm}^2$ [10]). In contrast to black silicon the ICP cryo etched pillars show regular shape and arrangement. A flat top area is visible on which wetting layers can be applied as a bonding agent. Finally, the uniform height of the pillars allows to find a uniform pressure for simultaneous bonding of all pillars of an array in a flip-chip process which is necessary for reproducible device fabrication [7].

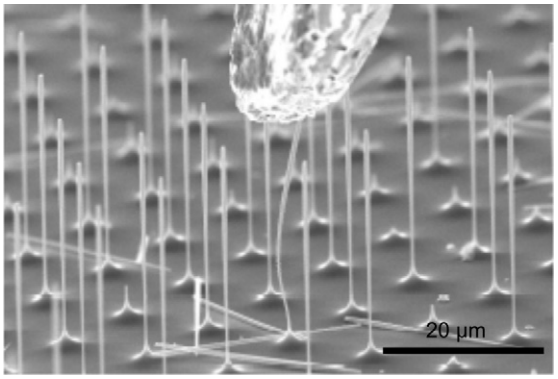

Fig. 6. SEM of a silicon pillar contacted by gold probe (pillar diameter 650 nm, height 34 μm, *n* doped silicon).

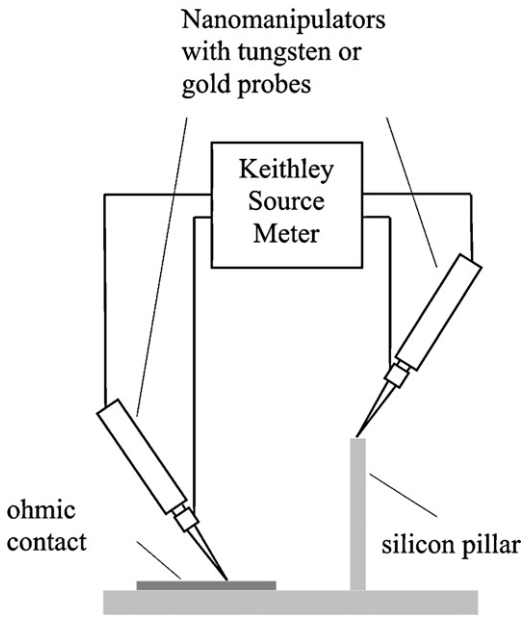

Fig. 7. Schematic of the measurement setup for the determination of the electrical conductivity of single silicon pillars in an SEM.

3. Electrical conductivity of silicon pillars

In order to estimate the suitability or efficiency of nanostructured silicon as a material for thermoelectrics, measurements of values that define the figure of merit Z were necessary. In the following measurements of the electrical and thermal conductivity of single silicon pillars are presented. For the determination of the electrical conductivity numerous I–V characteristics were recorded with individual pillars having approximately the same geometrical dimensions. Fig. 6 shows silicon pillars contacted by a gold-tip probe directly from above. The second large-area ohmic contact was outside of the pillar array (Fig. 7). The measurements of the electrical resistance of single pillars were done in a scanning electron microscope (SEM) equipped with nanomanipulators. The schematic structure of the measurement setup is shown in Fig. 7. After the probe was contacted with the pillar an electri-

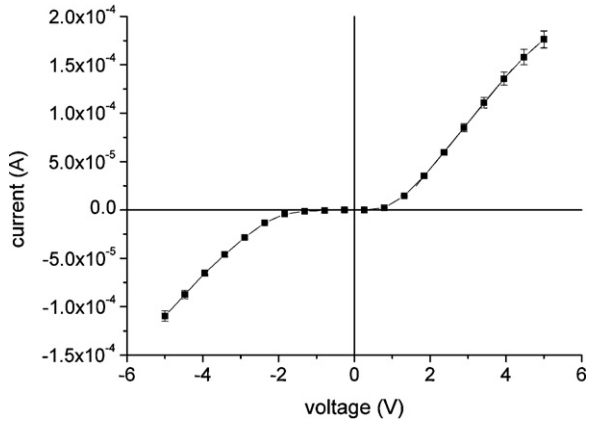

Fig. 8. *I–V* curve measured with silicon pillars (⌀ 650 nm, height 34 μm). Data points represent average values obtained with 5 pillars.

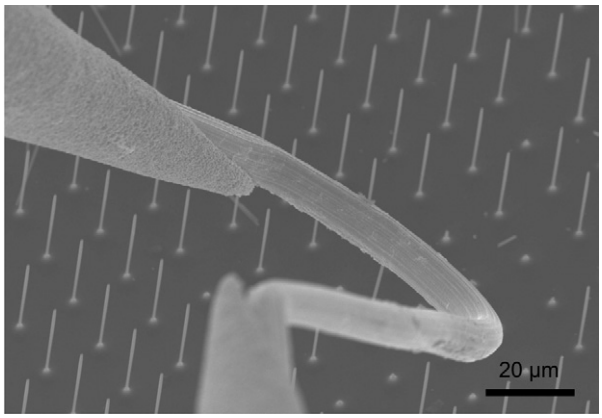

Fig. 10. SEM of a Wollaston wire in contact with a single silicon pillar.

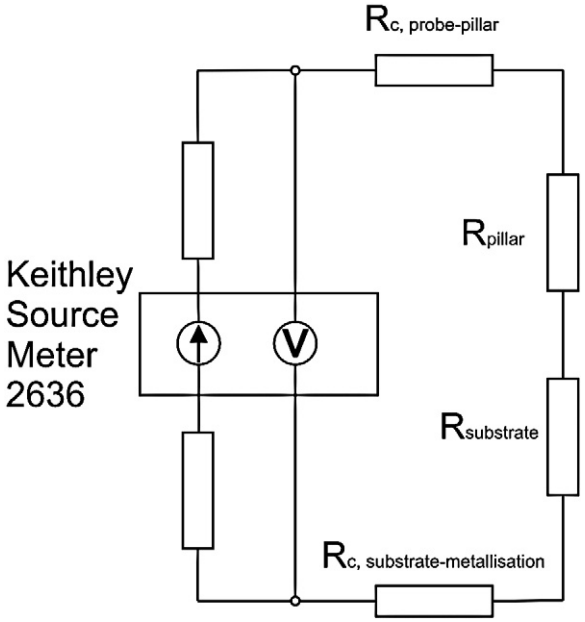

Fig. 9. Equivalent circuit of the measurement setup for the determination of the electrical conductivity of a single silicon pillar.

cal current was passed though the pillar and the resulting voltage between the probes was measured. This measurement was done using a Keithley SourceMeter 2600. Subsequently, the results were recorded and analyzed with a computer. Fig. 8 shows the average of 5 *I–V* measurements and the corresponding standard deviations. The shape of the curve shows the expected, typical characteristics of the top contact representing a Schottky contact. By linear fitting of the curve in the region between 2 and 4 V, we obtained a resistance of 21.2 kΩ. We performed four point probe measurements with the bulk silicon yielding an electrical conductivity of $69.8 \pm 2.7\,(\Omega\,\mathrm{cm})^{-1}$ which is well within the range between $50\,(\Omega\,\mathrm{cm})^{-1}$ and $125\,(\Omega\,\mathrm{cm})^{-1}$ specified by the wafer manufacturer.

In Fig. 9 the equivalent circuit diagram of the measurement circuit is shown. Assuming uniform conduction over the entire cross section of the pillar we are able to model the pillar resistance R_{pillar} based on the electrical conductivity of $69.8 \pm 2.7\,(\Omega\,\mathrm{cm})^{-1}$ of the employed wafer material. Using the measured dimensions of the pillars ($h = 34 \pm 2$ μm, diameter = 650 ± 8 nm) we calculate $R_{\mathrm{pillar}} = 14.7 \pm 1.8$ kΩ. Subtraction of the modelled from the measured pillar resistance yields a resistance of the two contacts and the substrate of 6.5 ± 1.8 kΩ. Assuming a typical specific contact resistance of $10^{-4}\,\Omega\,\mathrm{cm}^2$ for Cr/Au on n-doped silicon of a specific resistance of 0.01 Ω cm, we calculate a contact resistance of $R_{\mathrm{c,\ substrate\text{-}metallization}} = 2 \times 10^{-4}\,\Omega$ for the selected large contact area of 7 mm × 7 mm. As an estimate for $R_{\mathrm{substrate}}$ we take the spreading resistance below the pillar yielding a value of 76 Ω. Obviously, both resistances can be neglected compared to the resistance of the pillar, i.e. $R_{\mathrm{c,\ substrate\text{-}metallization}}, R_{\mathrm{substrate}} \ll R_{\mathrm{c\ probe\text{-}pillar}}$. With $R_{\mathrm{c\ probe\text{-}pillar}} \approx 6.5 \pm 1.8$ kΩ and assuming that the contact area extends over the entire top area of the pillar we obtain a specific contact resistance of $(2.0 \pm 1.8) \times 10^3\,\Omega\,\mu\mathrm{m}^2$. For device applications a reduced contact resistance is necessary which can be expected using a metallization layer [11].

To investigate the electrical conductivity in dependence on the pillar diameter the *I–V* characteristics of metallized *n*-doped silicon pillars with diameters of 500 nm, 700 nm, 1000 nm, 2000 nm and 5000 nm were measured and analyzed as described above. As expected according to [6] no decrease of conductivity was observed. Averaging yielded a value of $69.2 \pm 9.1\,(\Omega\,\mathrm{cm})^{-1}$, in very good agreement with the bulk electrical conductivity of the material measured using a four-point probe. Furthermore, these results confirm that the contact resistance of metalized pillars can be neglected. Measurements of the Seebeck coefficients of silicon pillars which are necessary to calculate *ZT* are in progress. From investigations with nanowires [6] we can expect an increase of the figure of merit *Z* by the same factor as the thermal conductivity decreases.

4. Thermal conductivity of silicon pillars

Thermal conductivity measurements with a large number (more than 100) of individual silicon pillars were made using the 3ω method in an SEM equipped with a nanomanipulator carrying a Wollaston wire probe, i.e. a platinum wire of 10 μm in diameter in thick silver cladding which had been removed over a length of 1.2 mm. In Fig. 10 the Wollaston wire brought into contact to the top area of a silicon pillar is shown. With this method the thermal conductivity of bulk material or thin layers can be determined [12]. The thermal wave generated by passing an alternating current at a frequency ω through the Wollaston wire penetrates into the contacted material depending on the thermal conductivity of the sample. This changes the temperature and thus the resistance of the wire. The temperature change in the wire occurs at a frequency of 2ω which can be measured using the 3ω voltage, i.e. the signal amplitude at the frequency of 3ω, which drops along the wire [13]. The frequency dependence of the real part of the complex oscillation amplitude

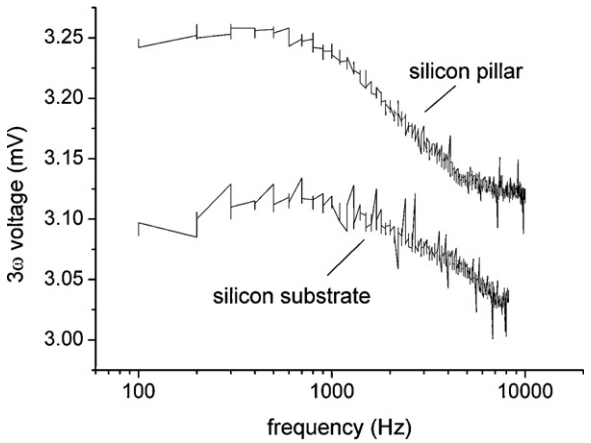

Fig. 11. 3ω voltage in dependence on frequency measured with a silicon substrate and a silicon pillar (⌀ 650 nm, height 34 μm), respectively.

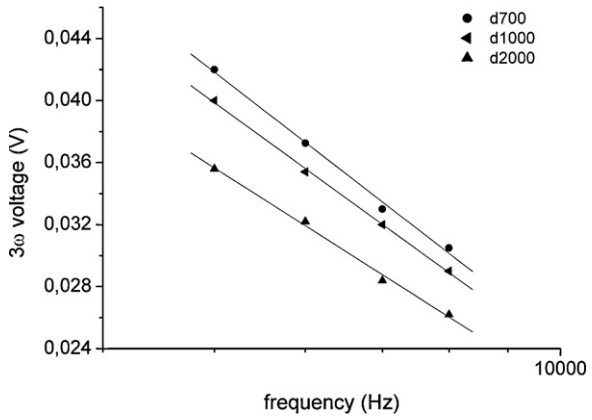

Fig. 12. 3ω voltage in dependence on frequency measured with silicon pillars of different diameters.

can be approximated by:

$$V_{3\omega} \propto \frac{1}{\kappa} \ln(\omega) \tag{1}$$

i.e. the 3ω voltage is inversely proportional to ln(ω) signal. The slope decreases with increasing thermal conductivity κ [13]. In this study we applied the Wollaston-wire-based 3ω method for the first time to silicon pillars. In Fig. 11 the 3ω signal measured with a silicon pillar of 650 nm in diameter is shown in comparison with 3ω signal measured with the bulk silicon wafer from which the pillar was fabricated. The much higher slopes of the curve taken with the pillar compared with the bulk silicon characteristic indicate that the thermal conductivity is much lower in the pillar than in substrate. A decrease of thermal conductivity with a reduction of dimensions, e.g. in a layer or a wire can be expected due to the increasing influence of phonon-boundary scattering. In a semiphenomenologocal approach Matthiessen's rule can be used to calculate the thermal conductivity κ of a nanopillar in dependence on its diameter d [14]:

$$\frac{1}{\kappa} = \frac{3}{Cv_g \Lambda} + \frac{3}{Cv_g d} \tag{2}$$

where Cv_g is the product of the heat capacity C and the group velocity v_g, Λ is the mean free path of phonons (=250 nm). A value of 1.7×10^9 W/m^{2}K was reported for the heat capacity-group velocity product which had been determined using empirical data from silicon nanowires.

To check the validity of this dependence for the pillar samples prepared in this study we performed 3ω measurements with pillars of different diameters. For these measurements a Wollaston wire of 5 μm in diameter was employed. In Fig. 12 the measured 3ω voltages for pillars of diameters of 700 nm, 1000 nm and 2000 nm in the frequency range of constant κ/ln(ω) slope are shown. We found slopes which depend on diameter according to the expectation. The largest slope occurs for the smallest pillars. To calculate κ from the measured slope of a pillar of arbitrary diameter we had to refer to a standard pillar of known κ for a calibration of our 3ω setup. For the constant slope-conductivity product we found 0.59 Wm^{-1} K^{-1} VHz^{-1} assuming a thermal conductivity of the 2000 nm pillars of 126 Wm^{-1} K^{-1} (cf. Eq. (1)). Then we can calculate thermal conductivities of 110 Wm^{-1} K^{-1} and 104 Wm^{-1} K^{-1} for the 1000 nm and 700 nm pillars, from the measured slopes of 0.054 VHz^{-1} and 0.057 VHz^{-1}, respectively.

The values of the thermal conductivity for this tree different pillar diameters are displayed as squares in Fig. 13. The curve calculated according to Eq. (2) is superimposed to the data points as a line. We see a very good agreement between the theoretical calculation and measured values. The relative deviation for

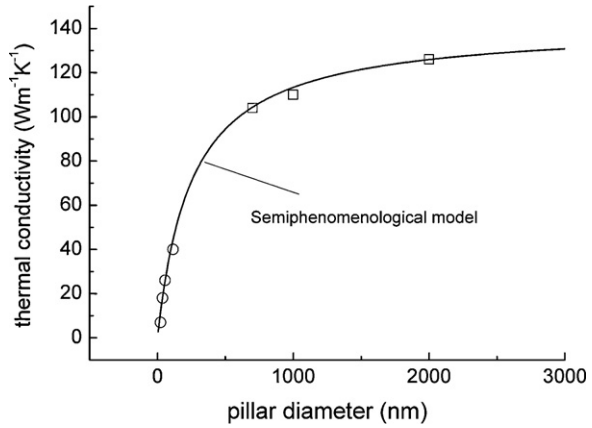

Fig. 13. Thermal conductivity in dependence on pillar diameter: calculation according to the semiphenomenological model (Eq. (2), solid line) and values of silicon pillars of different diameters derived from the measurements in Fig. 10 (open squares). Data points of silicon nanowires grown by the VLS method [11] were included for comparison (open circles).

1000 nm pillars is 2.7% and for 700 nm pillars 0.4%. Recently published values of the thermal conductivity of silicon nanowires were displayed as circles to support the semiphenomenological model [15].

The good agreement of the results of the present study with the semiphenomenological model shows that the thermal conduction behavior of silicon pillars fabricated using ICP cryo etching corresponds to that of silicon nanowires grown using a vapour–liquid–solid (VLS) process. Furthermore, the applicability of the Wollaston-wire-based 3ω method for thermal conductivity measurements with high-aspect ratio silicon pillars was confirmed. Measurements with the pillars of diameters down to 170 nm are lacking for which a Wollaston wire of 1 μm in diameter or less is in preparation. A thermal conductivity of less than 60 Wm^{-1} K^{-1} could be expected according to Eq. (2) which is a reduction of ×2.5 with respect to bulk silicon.

Our results indicate that thermal conductivity in ICP cryo etched pillars is limited by the same scattering mechanisms which dominate phonon transport in VLS silicon nanowires having a smooth surface. A drastic reduction of thermal conductivity can be expected if the surface roughness is increased [15]. ICP cryo etching offers both smooth 3D etching as well as the grey or black silicon etching regime which are combined to obtain high-aspect-ratio silicon pillars of defined surface roughness.

5. Conclusions

Fabrication and characterization of silicon pillars for thermoelectric devices were described. Top-down structuring of silicon wafers using ICP cryogenic dry etching was combined with thermal oxidation followed by oxide stripping in buffered HF solution for further reduction of the pillar diameter in the sub-micrometer regime. Electrical resistance and thermal conductivity of single pillars were measured in a scanning electron microscope equipped with nanomanipulators. A Wollaston-wire-based 3ω technique was used for the first time for thermal conductivity measurements with single silicon pillars. We found a reduction of thermal conductivity with the pillar diameter according a semiphenomenological model based on empirical results from silicon nanowires grown by the vapour–liquid–solid method. Investigations using a thinner Wollaston wire probe are in progress with silicon pillars having diameters less than 700 nm.

Acknowledgements

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Biographies

Andrej Stranz was born in Moscow, Russia, in 1977. He received the Diplom-Ingenieur degree in electrical engineering from Technical University Braunschweig, Germany in 2006. Since 2007 he is employed at Institute of Semiconductor Technology of the Technical University Braunschweig, Germany. Currently he is working as PhD student on the DFG project "Silicon-based thermoelectric nanosystems".

Ünsal Sökmen received in 2006 his diploma degree in materials engineering from Clausthal University of Technology, Germany. After that he joined to the Institute of Semiconductor Technology at Braunschweig University of Technology. His research interests include nano- and micromachining of silicon and compound semiconductors for the realization of microsensors and microactuators, and also developing of ICP cryogenic dry etching of silicon for MEMS and optoelectronic applications. His study is concentrated on fabrication and characterization of a silicon cantilever-based microbalance to weigh airborne nanoparticles.

Julian Kähler was born in Wilhelmshaven, Germany, in 1982. He received the Diplom-Wirtsch.-Ingenieur degree in industrial engineering with focus on German-Chinese business relationships and metrology for semiconductor sensors from the TU Braunschweig University of Technology, Germany in 2009. Since 2009 he is a PhD-student at the Institute of Semiconductor Technology of the Technical University Braunschweig, Germany. Currently he is working on joining techniques for high-temperature applications and on sensors for deep borehole drilling monitoring.

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